An Event Driven Read-Out System for a Novel PET Scanner With Compton Enhanced 3-D Gamma Reconstruction

A. Dragone, F. Corsi, C. Marzocca, P. Losito, D. Pasqua, E. Nappi, R. De Leo, J. Séguinot, A. Braem, E. Chesi, C. Joram, P. Weilhammer, F. Garibaldi, and H. Zaidi

***Abstract*—The design of a data acquisition system (DAQ) for a novel positron emission tomography (PET) scanner is reported. The PET system, based on long axially oriented scintillation crystals, readout by hybrid photon detectors (HPD), allows 3-D parallax-error free Compton enhanced gamma reconstruction. The DAQ system is composed of several readout cards, each one associated with a module of the PET scanner, and of a main card that controls the whole system. Using fast triggering signals from the silicon sensor back-planes, the main card performs the coincidence analysis and, in case of coincidence, it enables the readout of the two modules involved. The other modules are left free to perform new acquisitions. This concept based on several independent, event-driven and parallel readout chains, drastically reduces the acquisition dead time. Each enabled readout card digitizes, encodes and stores data from the associated module. Data are stored in a local FIFO and then are transferred through a network into a single computer. The system is designed according to the specifications of the IDEAS VaTaGP5 chip. Each readout card is able to accommodate all the chip readout modes and the test procedures and can be used as a standalone readout system that allows reading out up to 16 daisy chained chips per channel. The DAQ system here reported, designed for a two module demonstrator setup, was developed to study and optimize the essential design parameters.**

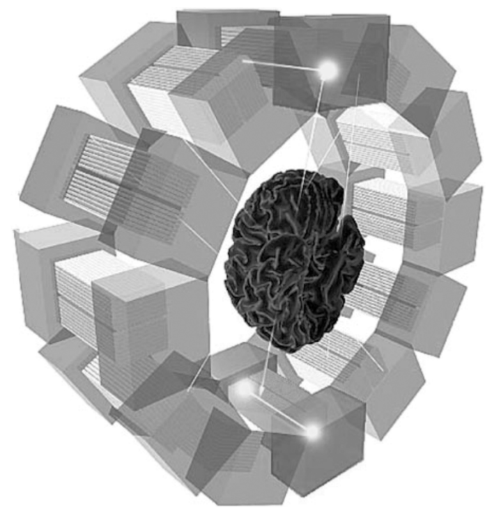

Fig. 1. 3-D geometrical model of the novel PET scanner.

I. Introduction

POSITRON emission tomography (PET) is widely recognized as the least invasive molecular imaging technique [1]–[3]. Its main features include sensitivity to tracer concentrations of picomole level and the ability to provide information on metabolic and kinetic molecular processes for both detection and treatment of major diseases. The large number of channels present in the detectors and the high rates characteristics of this technique, call for fast and parallel processing capabilities, typically achieved with the implementation of dedicated application specific integrated circuits (ASICs). This leads to high costs and long development times. The extensive use of field programmable gate arrays (FPGAs) could represent a good compromise between cost and complexity, allowing faster circuit realization and, at the same time, the implementation of reconfigurable electronics functionality to support system configuration, self calibration, test and future firmware improvements.

In this paper we report on the design of a DAQ system for a 3-D PET scanner based on a novel geometrical concept which aims at optimizing the performance in terms of sensitivity, spatial resolution and image contrast. The scanner is composed of 16 detector modules arranged in a ring (Fig. 1).

The DAQ system is composed of three kinds of cards: the back-plane cards (BP), the readout cards (RO) and the process controller card (CP). The BP cards extract the triggering signals from the module detectors (FORMs = Fast OR signals from a module) and process them in order to detect only meaningful events, while the RO cards performs the readout of the modules. The CP card controls the synchronization of both the BPs and the ROs cards and manages the data transfer into a server-like workstation through a network with a suitable data transfer protocol. In order to reduce drastically the acquisition dead time and the detection of accidentals, the DAQ system is organized in several independent event driven and parallel readout chains controlled by FPGAs with real-time processing capabilities. In particular the one that performs the coincidence analysis is able

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A. Dragone, F. Corsi, and C. Marzocca are with the Electrics and Electronics Department, Politecnico di Bari, 70125 Bari, Italy (e-mail: dragone@deemail.poliba.it; corsi@poliba.it; marzocca@poliba.it).

P. Losito and D. Pasqua are with the Microlaben s.r.l., 70125 Bari, Italy (e-mail: p.losito@microlaben.com; d.pasqua@microlaben.com).

E. Nappi and R. De Leo are with the INFN Bari, 70126 Bari, Italy (e-mail: Eugenio.Nappi@ba.infn.it; raffaele.deleo@ba.infn.it).

J. Séguinot is with the Collége de France, 75231 Paris, France (e-mail: Jacques.Seguinot@cern.ch).

A. Braem, E. Chesi, C. Joram, P. Weilhammer are with the PH Department, CERN, 1211 Geneva 23, Switzerland (e-mail: Andre.Braem@cern.ch; Enrico.Chesi@cern.ch; Christian.Joram@cern.ch; Peter.Weilhammer@cern.ch).

F. Garibaldi is with the Istituto Superiore di Sanità, 00161 Rome, Italy (e-mail: Franco.Garibaldi@iss.infn.it).

H. Zaidi is with the Division of Nuclear Medicine, Geneva University Hospital, 1211 Geneva 14, Switzerland (e-mail: habib.zaidi@hcuge.ch).

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Fig. 2. 3-D model of a single module composed of a scintillator matrix and two HPDs.

to discriminate a substantial fraction of accidental, meaningless events avoiding their processing [4]. This results in a significant reduction of the amount of data to be transferred and stored, allowing the use of commercial PC workstations and a faster post-processing. The reduction of accidental coincidences also improves the image quality.

II. 3-D PET Scanner Architecture

The 3-D axial PET scanner, fully described in previous works [4]–[6], consists of several identical modules. A module (Fig. 2) comprises a matrix of long axially oriented scintillator crystals, which are readout on both sides by hybrid photon detectors (HPDs) [7] with integrated front-end electronics.

This structure provides a full three-dimensional reconstruction of the two 511 keV gamma quanta from the positron annihilation. The axial arrangement of the scintillating crystals is a natural and straightforward idea to suppress the parallax error which is inherent to all radial geometries. Such idea was already proposed for Positron CT applications in 1988 [8]. Limits of this first proposal and difference with the present one are discussed in [4].

The highly segmented geometry of the silicon sensor, inside the HPD, provides an accurate and uniform spatial resolution in the transaxial (x-y) plane, completely independent of the radial detector thickness. The axial coordinate (z) of the interaction point is derived with good precision from the ratio of the light intensities detected by the two HPDs at the ends of each scintillator matrix. This leads to a full 3-D image reconstruction without any parallax effect and with a spatial resolution which is almost constant over the full field of view. The transaxial segmentation allows tracking of multiple interactions of annihilation photons in the scintillator matrix and thus allows the reconstruction of a fraction of events (estimated around 15%) which underwent Compton scattering in the detector. The fact that a substantial fraction of Compton events scattered in the detector can be unambiguously reconstructed, turns into an enhanced sensitivity of the PET system.

Both the crystals and the HPD are key components of the system. The crystals influence the resolution of the system. Whereas the x-y coordinate resolution depends only on the crystal segmentation and not on its constituent materials, the z resolution is instead linked to the choice of the scintillator and to its properties. In particular the two characterizing parameters are the light yield and light absorption length. In the first phase of the project aimed to build a demonstrator, YAP:Ce crystals have been chosen for their low cost, even if, compared to other scintillators, YAP features a low Z, a high absorption length, and a low photofraction [5]. Tests on these crystals have been carried out to measure the light attenuation length of YAP:Ce crystals as a function of different coatings of the lateral surfaces of the scintillator bars [9]. An energy resolution of about 10% (FWHM) is expected. LYSO crystals will be tested and used in the final system as described in previous works [4].

The HPDs designed for the PET prototype camera have a circular thin entrance window made of sapphire and are equipped with semi-transparent bialkali photocathodes, which exhibit a quantum efficiency of about 25% at 370 nm. The electron optics of the HPD is such that a 1:1 image of the photon pattern on the photocathode is transferred to the silicon sensor ("proximity focusing"). The silicon sensor is segmented into 208 individual diodes of dimension 4x4 mm ^{2} matching the pattern of the crystals matrix (16 $\times$ 13). The HPD, operated at a moderate potential difference between the photocathode and the silicon sensor, provides a gain of about 3000. The integrated self-triggering electronics, the VLSI ASIC VaTa-GP5 [10], fabricated in 0.6 μm CMOS technology, is mounted on the ceramic carrier, which supports also the silicon sensor. Each of the 128 channels of this chip has a charge integrating preamplifier, a shaper and a readout register. Each channel includes also a parallel fast shaper circuit ($\tau_{\rm s} = 50$ ns) followed by a discriminator that produces a trigger signal for the readout logic. Unlike previous VA versions, the ASIC features different readout modes: serial readout, sparse readout, sparse readout with adjacent, and random access readout [10], [11]. When multiple triggered channels occur, the sparse readout option, instead of reading out all the channels serially, allows reading out only the triggered ones. Thus, this readout mode can sustain event rates on the order of several MHz and so it is suitable for the typical rates of PET applications.

III. Data Acquisition System

The data acquisition systems (DAQs) for PET cameras need to cope with high single and coincidence count rates as well as high data taking rates. Our approach, tailored to the specific characteristics of the HPD front-end electronics, features a readout card (RO card) and a back plane card (BP card) per module and a common main card that controls the system (CP). The RO cards are coupled to a single common high density storage medium. The DAQ working principle and its features

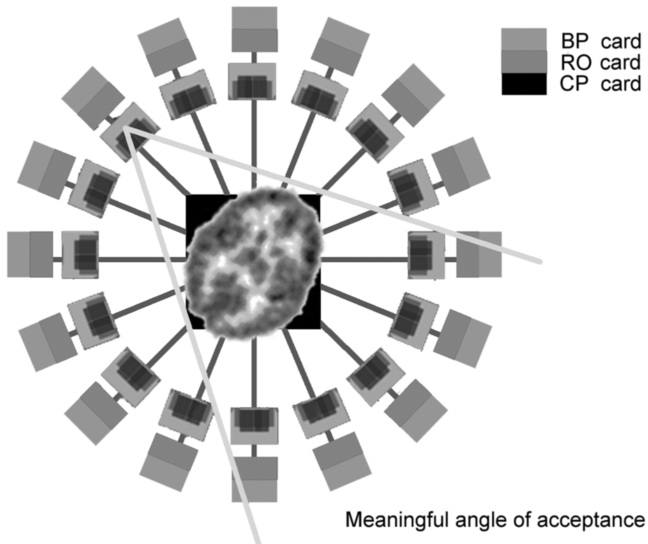

Fig. 3. Geometrical acceptance range, in which coincidences can be formed, is defined for each module.

are driven by three main constraints: (i) the requirement to perform coincidence check in small time windows, (ii) the tradeoff between the need of parallelism, due to high event rates, and the limits imposed by the technology on the maximum transfer rate into a data storage unit, and (iii) the requirement to detect and analyze gamma interactions, which involve, both total photoelectric conversion and Compton scattering in the detector [4], [12].

A "good" PET event is defined as the time-coincident detection of two annihilation quanta of 511 keV energy emitted in a back-to-back configuration. Coincidences are formed on the level of camera modules. The counting rate of each module under the test conditions of the NEMA-NU2 protocol with a cylindrical phantom (20 cm diameter and 20 cm length) of 13 kBq ml^{-1} activity (total activity $=$ 81.4 MBq) is about 1.8 MHz. In order to reduce the probability of accidentals, the determination of an event should be done in a coincidence time window (CTW) as narrow as possible. The minimum time window will depend on the jitter among the FORMs of the HPDs (2–3 ns). Furthermore, events must be tracked in a unique CTW shared among the modules. In other words, the CTW started by a generic event must be closed exactly at the same time for all the modules. On the contrary, allowing each module to start its own time window would imply that good events could be lost or false coincidences could be detected. For these reasons FORMs signals from each module are all propagated on matched lines to a single processing unit, the CP, that starts a time window as soon as one of these signals arrives and closes it after the time interval in which the system performs the coincidence analysis. When a coincidence is detected (i.e., only two modules within a meaningful angle of acceptance have sent the FORM signal during the CTW), the readout of the previous two modules begins. The definition of a meaningful angle of acceptance allows to reduce the detection of accidental false coincidences, discarding the geometrical configurations without a physical meaning [12] (Fig. 3). Only the couple of modules that fulfill a coincidence in the CTW (if they exist) are read out, while the other modules are immediately reset, in order to be ready to accept coincidences with different modules. Two modules in coincidence define a chain, and chains are set dynamically by the CP card on the basis of the coincidence analysis.

To take into account the problems raised by the second constraint, the DAQ system should be able to readout modules in parallel, in order to minimize the dead time between subsequent acquisitions. Different levels of parallelism have been implemented. At the first level, two modules in coincidence, i.e., a chain, are readout in parallel (one RO card per module).

At the second level, chains are read out in "parallel" because when a chain is set and goes through readout, other chains can be set and go through readout among the free modules. On the other hand, the higher is the grade of parallelism the higher is the data rate that has to be faced by the storage unit. A good compromise was achieved by reading out in parallel only modules in coincidence. This approach leads to a scheme that features several independent event driven and parallel readout chains and therefore reduces drastically the acquisition dead time and the detection of accidentals (Fig. 4).

This scheme is intrinsically limited by the fact that when a coincidence between two modules is detected a suitable signal must be provided to the front-end in order to avoid the generation of triggers from other channels before completing the readout. VaTaGP5 used in sparse readout mode, offers the solution to the problem by using the disable late trigger (DLT) function. Since the DLT signal can be generated only after the end of the coincidence analysis and considering the delay time of the cables between the cards, it is impossible to use this function to select only one single event. To address this issue, signals derived from the HPDs silicon back plane are acquired by dedicated cards, the BP cards. For a single 511 keV event, a low-impedence high-bandwidth amplifier with a 5 ns shaping time is able to sense $1/3$ of the total charge generated in the detector. This fast signal can be used to generate the FORM instead of the triggers produced by the VaTaGP5 chips. Even considering the delay introduced by the cables plus the duration of the CTW, the enabling DLT signal, generated by the CP after an event happens, can arrive at the BP card well before the generation of the trigger due to the same event and the DLT can be applied after a suitable delay in order to select that single event.

The third constraint requires running the FE electronics with a relatively low detection threshold (50 keV) in order to detect and reconstruct the recoil electron of the primary Compton scattering. However, the low threshold prevents the rejection of a large fraction of gammas which underwent Compton scattering in the organic tissue and this turns into technically unfeasible DAQ rates. The problem can be solved considering that signals derived from the HPDs silicon back plane, which, as they cover the full detector area, are proportional to the total energy converted in the scintillator block. Thus, if the back plane signals are compared with a suitable energy window in order to identify and reject low-energy gamma rays (after Compton scattering in the patient), the ability of the FE electronics to detect Compton interactions in the scintillator matrix is not compromised.

In the following paragraphs, a detailed description of the cards functions and components is reported.

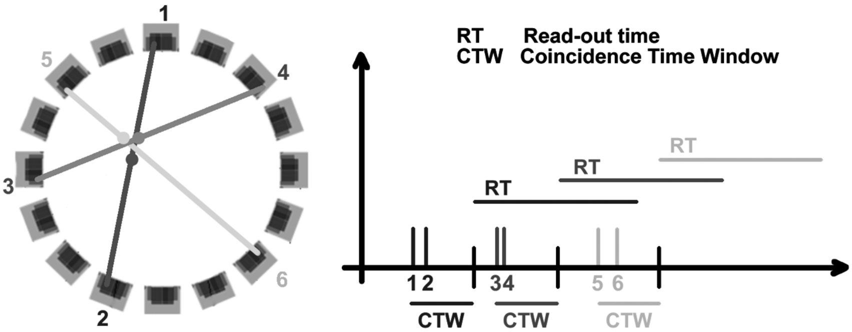

Fig. 4. Example of three parallel chains.

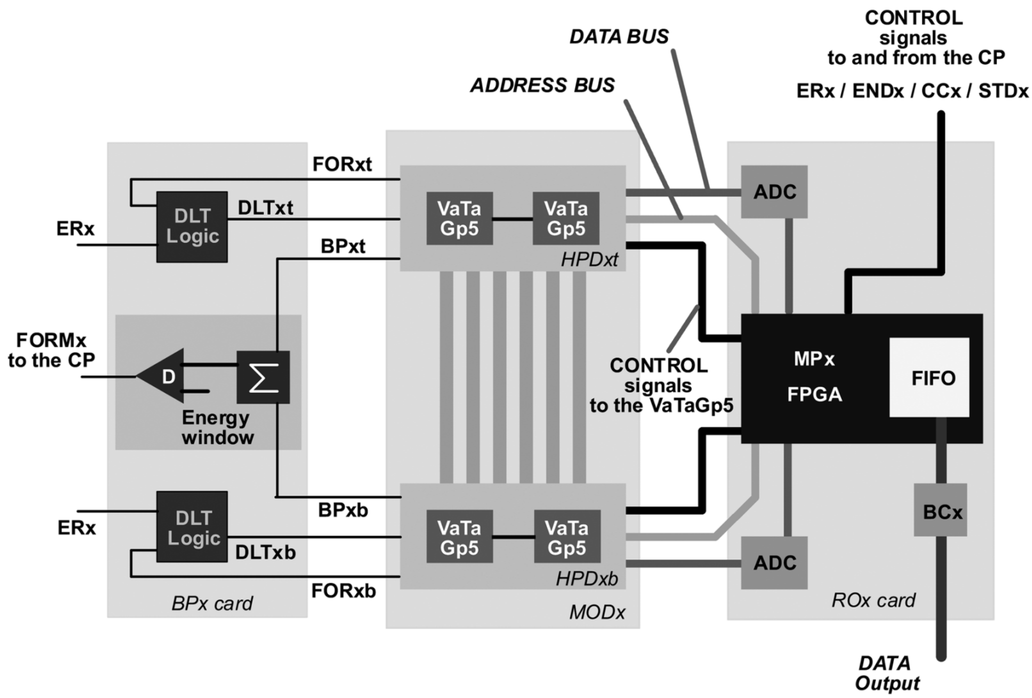

Fig. 5. Schematicrepresentation of the signal data flow between a module and the corresponding BP and RO card.

A. Back-Plane Card (BP Card)

The BP card (Fig. 5 - left) has three main components: the amplifiers, the analog adder, and the DLT logic.

The amplifiers sense the back planes of the HPDs of a module and generate the back plane signals. In order to compensate for the nonlinearity in the light absorption along the scintillator bars, a suitable weighted analog sum [4] is performed in a summation block and the signal is sent to a double threshold discriminator that generates the FORM. The BP card features also a DLT logic, needed (i) to apply the DLT signal to the front-end when the ER signal, which enables the readout, arrives from the CP and (ii) to reset the front-end in a self reset mode. When no ER signal arrives, a trigger from the HPD (FOR) can be generated only by a false or accidental events which must be rejected, and it is used to self reset the VaTaGP5 chips.

B. Read-Out Card (RO Card)

The RO card (Fig. 5 - right) digitizes, encodes and stores data from the respective module. When enabled from the CP (ER), the module processing logic (MP) implemented in FPGA performs the readout of the two HPDs of the module in parallel, according to the sparse readout mode procedure of the VaTaGP5 chips. Two 3-stage, 12 bit pipeline flash ADCs are used to digitize analog data. Once the data have been acquired and stored in an internal FIFO buffer, the MP logic performs a coincidence check in order to verify that only one event has been detected and sets a corresponding coincidence check flag (CC). The MP logic then sets an end readout flag (END) high and waits for an acknowledgment from the CP card before transferring the data through a network into a single server-like computer exploiting a fast data link. For the two module demonstrator USB2.0 connections have been implemented to connect the RO cards to a standard PC. Each readout card is equipped with all the necessary circuitry needed to provide the biasing signals and the control signals required by the VaTaGP5 chips [10], [13]. Furthermore, it can accommodate all the readout modes and the test procedures of the front-end chip and it can be used as a stand-alone readout system that allows reading out up to 16 daisy chained chips per channel (2×16). The two independent channels are

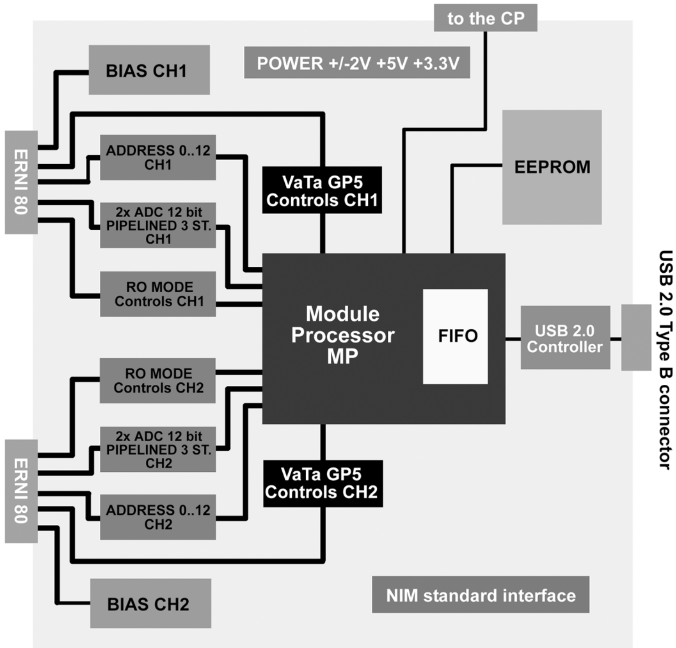

Fig. 6. Schematic representation of the RO card.

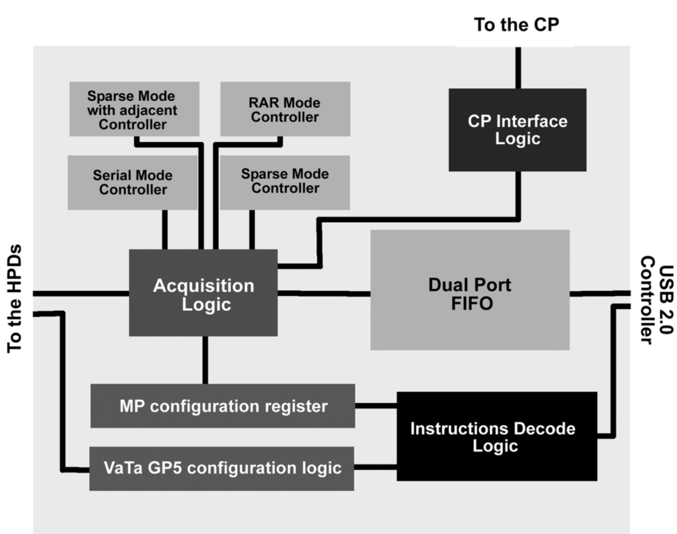

Fig. 7. Schematic representation of the MP logic.

readout in parallel. A more detailed schematic of the RO card, designed for a two module demonstrator setup, is reported in Fig. 6 and a block schematic of the MP logic is shown in Fig. 7.

C. Process Controller Card (CP Card)

The CP card has a single component, the process controller implemented in FPGA. The CP logic (Fig. 8) features a first section that senses the FORMs from the modules and enables the CTW timer. FORMS are then stored and counted within the CTW in order to detect coincidences.

When two modules are found in coincidence, a busy flag is set on them and LOR logic performs the combinatorial selection of meaningful line of records (i.e., lines between modules representing groups of lines between crystal bars). If the modules

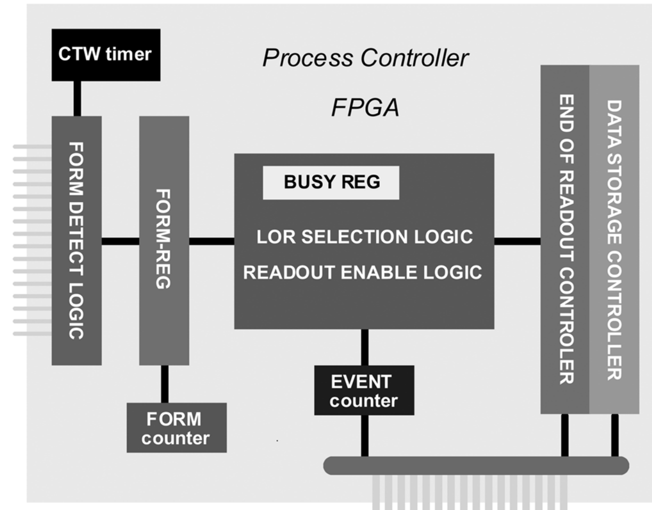

Fig. 8. Schematic representation of the CP logic.

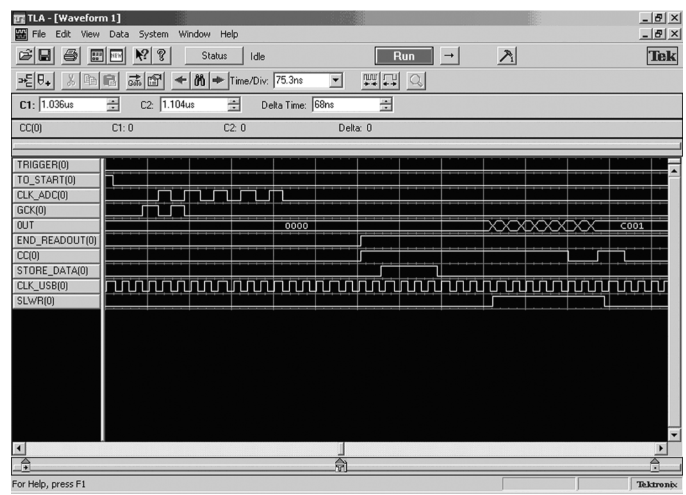

Fig. 9. Time diagram of the behavior of the MP acquisition logic.

are within a meaningful angle of acceptance, an event number is assigned to them and they go through readout. In order to start the data acquisition, the CP sends the ER signal and the event number (EN) to the corresponding RO cards. Then it resets the FORM register to perform subsequent analysis on the remaining free modules. The last section of the logic controls the storage of the data. When an END signal arrives from two modules in coincidence, the CP cross-checks the CC signals in order to check for a valid coincidence on both modules, then sends the store data signals (STD) to the relative RO cards. Otherwise, it resets the RO cards.

IV. Logic Tests

Logic tests have been performed in order to verify the behavior of the implemented readout modes. Digital signals from the detector have been simulated at the inputs of an Altera Stratix Pro evaluation board in which the logic was loaded. Output signals from the FPGA have been monitored by a Tektronix TLA601 logic state analyzer. As an example, the time diagram in Fig. 9 shows the behavior of the MP acquisition logic measured with the analyzer.

V. Conclusion

A compact event-driven DAQ system with a high grade of parallelism and a fast storage system has been designed. The system has been studied for a novel kind of PET, based on the hybrid photon detectors, that allows the detection and reconstruction of Compton scattered events and, at the same time, a 3-D image reconstruction without any parallax effect. This results in an enhanced sensitivity and in a spatial resolution which is almost constant over the full field of view. The system is modular and reconfigurable through the FPGA in each single card using a single common data link from the main external host computer. The logic of the system has been implemented and tested with an Altera Stratix Pro evaluation kit. A DAQ system for a two module demonstrator is under construction to demonstrate the feasibility of the whole system.

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